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4. Title of the invention
SEMICONDUCTOR DEVICES WITH INCREASED BREAKDOWN VOLTAGE

5. Name of your agent (*if you have one*)

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SEMICONDUCTOR DEVICES WITH INCREASED BREAKDOWN VOLTAGE

The breakdown reverse voltage of known simple semiconductor (pn junction) diodes (see Fig. 1a) is strongly related to the allowed maximum electric field (about 0.2 MV/cm for silicon). The breakdown voltage depends therefore on the concentration of the equilines of voltage within the edges of the depletion layer to either side of the pn junction, and thus the extent of the depletion layer, which depends on the doping levels at both sides of the pn junction.

The direct relation between doping level and breakdown voltage as occurring in the simple diode shown in Fig. 1a of the accompanying drawings can be circumvented by a variety of known structures all using what is well known as the RESURF mechanism.

One example of a document disclosing RESURF mechanism structures is US Patent No. 4,754,310 (our reference PHB32740), the contents of which are hereby incorporated by reference. In this US Patent examples are disclosed of power devices including rectifier diodes, field effect transistors and bipolar transistors. In the case of a simple rectifier diode there is a structure which is equivalent to that shown schematically in Fig. 1b of the accompanying drawings. In the structure shown in Fig. 1b the electric field and the depletion layer are stretched over a larger distance to either side of the pn junction at the same reverse voltage. This leads to higher breakdown voltages. The major problem in Fib. 1b is that there has to be a very good balance of P and N doping.

In US Patent No. US-A-4,754,310 a trade off relationship between the on-resistance and the breakdown voltage of a field effect transistor is addressed by providing the drain drift region as a zone formed of first regions of one conductivity type interposed with second regions of the opposite conductivity type, in similar manner to the alternating p type and n type zones shown for a diode in Fig. 1b of the accompanying drawings, with the dopant concentrations and dimensions of the first and second regions being such

that, when the device is operated in voltage blocking mode and the zone is depleted of free charge carriers, the space charge per unit area in the first and second regions balances at least to the extent that the electric field resulting from the space charge is less than the critical field strength at which avalanche breakdown would occur in a 1D diode (or drain drift region) having the same dopant concentration. This enables the required reverse breakdown voltage characteristics to be obtained using interposed semiconductor regions which individually have a higher dopant concentration, and thus lower resistivity, than would otherwise be required so that the series resistivity of the first and second regions and thus the on-resistance of the device can be lower than for conventional devices.

For best results in a field effect transistor using the invention of US-A-4,654,310 the charge balance between each pole in the drain drift region needs to be precise. That is to say the integral of the doping concentration perpendicular to the junction of the two interposed regions of one conductivity type and opposite conductivity type needs to have the same value of about $2x10^{12}cm^{-2}$. Doping concentration to this level of precision in integrated circuit processing techniques is difficult, and a small fluctuation in doping concentration in either of the two regions results in a correspondingly large deviation from the desired charge balance along the drain drift region and a corresponding large reduction in the reverse breakdown voltage of the device.

International patent application published as W001/59847, the contents of which are hereby incorporated herein by reference (our reference PHNL 000066) provides another way of improving the trade off between breakdown voltage and on resistance in the case of vertical high voltage insulated gate field effect devices. Field shaping regions extend through the drain drift region from the body regions of the device to the drain region. These field shaping regions are semi-insulative or resistive regions which provide current leakage paths from the source regions when the device is non-conducting and a voltage is applied between the main electrodes of the device so as to cause an extension of a depletion region in the drain drift region towards the drain region to increase the reverse breakdown voltage of the device. The small

leakage current along the resistive paths causes a linear electrical potential drop along these paths. Hence a substantially constant vertical electric field is generated along these paths and accordingly in the adjacent drain drift region, and this results in the breakdown voltage being greater than for a non-uniform electric field which would occur in the absence of the field shaping region. Thus, as for the invention of US-A-4,754,310, for a given required breakdown voltage of the device, it is possible to increase the doping concentration of the drain drift region and hence reduce the on-resistance of the device compared with a conventional device.

International patent application published as W003/015178, the contents of which are hereby incorporated herein by reference, (our reference PHNL010570) discloses a bipolar transistor structure, comprising: a collector including a higher doped collector region of semiconductor material of a first conductivity type doped to a first concentration; an emitter region of semiconductor material of the first conductivity type; a base region of semiconductor material of a second conductivity type opposite to the first conductivity type between the emitter region and the collector; the collector further including a lower doped drift region extending between the higher doped collector region and the base region, the drift region being of the first conductivity type and doped to a second concentration lower than the first concentration; a trench extending adjacent to the drift region; and a gate within the trench insulated from the drift region for controlling the drift region to be depleted of carriers in a voltage blocking mode of operation. The drift region in the collector is of lower doping concentration than the higher doped region of the collector so that the drift region may be depleted of carriers. Using the gate in the trench the drift region can be depleted even with a higher doping in the drift region than would otherwise be possible. This allows the product of the cut off frequency and the breakdown voltage to be increased as compared with prior art structures. Conveniently, the structure may be a vertical structure formed on a semiconductor body having opposed first and second faces. The emitter region may be connected to the first face and the collector region to the second face. The trench may extend substantially perpendicularly to the

first face through the emitter and base regions to the drift region. In alternative embodiments, a lateral structure may be provided, for example using an insulated buried layer as the gate. The gate may be of a semi-insulating material, and the structure may further comprise a first gate connection at the end of the gate adjacent to the boundary between the drift region and the base region and a second gate connection at the boundary between the drift region and the higher doped collector region. This allows a uniform field to be applied along the gate thereby providing a uniform field in the drift region to minimise the risk of breakdown at low voltages. The uniform field is achieved without complex doping profiles in the drift region being necessary.

Co-pending UK Patent Application No. 0221839.4 (our reference PHNL020937) concerns an invention in which there is provided a field effect transistor semiconductor device comprising a source region, a drain region and a drain drift region, the device having a field shaping region adjacent the drift region and arranged such that, in use, when a reverse voltage is applied between the source and drain regions and the device is non-conducting, a substantially constant electric field is generated in the field shaping region and accordingly in the adjacent drift region, characterised in that the field shaping region is arranged to function as a capacitor dielectric region between a first capacitor electrode region and a second capacitor electrode region, the first and second capacitor electrode regions being adjacent respective ends of the dielectric region and having different electron energy barriers.

By substantially constant electric field it is meant therein that the maximum electric field in the field shaping region and hence in the adjacent drift region at a given voltage is reduced in comparison with the absence of the field shaping region with the consequence that the breakdown voltage of the device is comparatively greater. Associated with the reduced maximum electric field is an increased integral of the electric field along the length of the field shaping region and the drift region and hence the greater breakdown voltage. It is possible to have a perfectly uniform electric field along both the field shaping region and the adjacent drift region but that depends on a number of factors including the device geometry, for example the extent of the

field shaping region along the length of the drift region and the extent of influence of the field shaping region across the width of the drift region.

In a device according to this co-pending UK Application invention, it is the different electron energy barriers of the first and second capacitor electrode regions which ensure that in use, when a voltage is applied between the source and drain regions and the device is non-conducting, the field shaping region functions as a capacitor dielectric region rather than a resistive region, there is substantially no space charge in the field shaping region, and within the drift region there is a charge balance between the space charge in the first capacitor electrode region, together with the drain drift region, and the second capacitor electrode region. That is to say, the charge in the drain drift region plus the charge in the first capacitor electrode region compensates the charge of the second capacitor electrode region. It is an applied voltage which capacitively generates the substantially constant electric field in the field shaping region in that invention rather than the leakage current applied through the field shaping region which is provided in the arrangement disclosed in W001/59847. Also, the problem with the arrangement of US-A-4,754,310 of providing a precise charge balance between the two opposite conductivity type regions along the length of the drift region does not arise in the arrangement of the co-pending UK Application.

In a device according to the invention of this co-pending UK Application, the field shaping region is described as being intrinsic semiconductor material, or being extrinsic semiconductor material which is lower doped than the drift region, or being semi-insulating material, for example comprising one of oxygen doped polycrystalline silicon and nitrogen doped polycrystalline silicon. The first capacitor electrode region may be a semiconductor region of one conductivity type with the second capacitor electrode region being a semiconductor region of opposite conductivity type to the first capacitor electrode region. In this case the different electron energy barriers of the first and second capacitor electrode regions are provided by the different work functions of the two semiconductor conductivity types. Alternatively, the first capacitor electrode region may be a semiconductor region with the second

capacitor electrode region being a Schottky barrier region. In this case the work function of the first capacitor electrode semiconductor region is an electron energy barrier which is different from the Schottky electron energy barrier of the second capacitor electrode Schottky barrier region. In both cases as just specified, the first capacitor electrode region semiconductor region is of the same conductivity type as the drain region. The transistor may be an insulated gate field effect transistor. This may be a vertical transistor which may be a trench-gate transistor.

The invention of W001/59847 discussed above is disclosed in relation to vertical high voltage insulated gate field effect devices. The vertical trench-gate transistor devices in accordance with the invention of UK Application No. 0221839 may also be high voltage devices, that is with breakdown voltages above about 100 volts, where the on resistance of the device is mainly determined by the resistance of the drain drift region. However, these vertical trench-gate devices may also be medium or low voltage devices, that is with breakdown voltages respectively below about 100 volts or below about 50 volts.

In a device according to the invention of UK Patent Application No. 0221839 where the transistor is an insulated gate field effect transistor, this may be a lateral transistor having the source region, the drain region and the drift region underneath a top major surface of the device, wherein a planar insulated gate is above said top major surface, and wherein the capacitor dielectric region and the first and second capacitor electrode regions are above said top major surface. Alternatively, the insulated gate field effect transistor may be a lateral transistor having the source region, the drain region and the drain drift region underneath a top major surface of the device, wherein the drain drift region is divided into laterally spaced sections, and wherein the capacitor dielectric region is underneath the top major surface and is divided into laterally spaced sections which alternate with the drain drift sections. In this case, the insulated gate may extend below the top major surface at the end of the drain drift sections opposite the drain region, or a planar insulated gate may be above the top major surface.

The field effect transistor devices according to the invention of UK Patent Application No. 0221839 may be used in direct current power applications. They may also be used in radio frequency power applications. The effect of the field shaping region is not only to enable the on resistance of the device to be decreased for a given breakdown voltage which is important for DC power applications, but also to increase the cut off frequency for a given breakdown voltage which is important for RF applications. Also, the fact that the field shaping region functions as a capacitor dielectric region rather than a resistive region (as is the case for example in W001/59847), and that there is substantially no space charge in the field shaping region when a voltage is applied between the source and drain regions, improves the switching speed of the device which is important for RF power applications. In the case specified above where the second capacitor electrode region is a semiconductor region, then the switching speed may be improved by choice of the type of semiconductor for this second capacitor electrode region, for example by choosing silicon-germanium rather than silicon. Furthermore, the switching speed is improved in the case specified above where the second capacitor electrode region is a Schottky barrier region rather than a semiconductor region. Where the devices are insulated gate field effect transistor devices as specified above, then the above-specified lateral transistor devices are particularly suitable for RF applications.

In a device according to the invention of UK Patent Application No. 0221839, instead of the transistor being an insulated gate field effect transistor it may be a Schottky gate field effect transistor. Schottky gate field effect transistors are known to be suitable for RF applications. The Schottky gate field effect transistor may be a vertical transistor. Alternatively this transistor may be a lateral transistor having the source region, the drain region and the drain drift region underneath a top major surface of the device, wherein the Schottky-gate is above said top major surface, and wherein the capacitor dielectric region and the first and second capacitor electrode regions are above said top major surface.

In the above-mentioned examples of a device according to the

invention of UK Application No. 0221839, the first capacitor electrode region may be integral with the drain region.

According to the present invention a semiconductor device with a semiconductor region having a pn junction has a field shaping region consisting of an insulating/dielectric material located adjacent to the semiconductor region pn junction, the field shaping region being arranged to be capacitively coupled to substantially the same voltages as are applied in use to both sides of the pn junction such that, when a reverse voltage is applied across the pn junction and the device is non-conducting the capacitively coupled insulating field shaping region induces a stretched electric field in the semiconductor region and limited to the depletion region as formed at the pn junction in the semiconductor region to increase the reverse breakdown voltage of the device.

The meaning of "coupled to substantially the same voltages" in the above definition of the present invention will be apparent from the description and explanation of the illustrated examples which follows. However, by way of brief explanation, it is noted here that the field shaping region may simply be directly coupled only to the same p and n semiconductor regions which form the pn junction; or the field shaping region may be coupled at one side to a p+ region adjacent the p region and/or at the other side to an n+ region adjacent the n region; or the field shaping region may be coupled to both p+ and p regions on one side and/or to both n+ and n regions on the other side; or the field shaping region may be coupled at one or both sides to an electrode (for example metal or highly doped poly silicon) which may be provided for this purpose or which may be a main or control electrode of the semiconductor device.

In devices according to the present invention the field shaping region adjacent the semiconductor pn junction may bridge the pn junction or it may be adjacent only one side of this pn junction. The field shaping region may be directly adjacent the semiconductor region having the pn junction or there may be an intervening passivation liner, that is a thin insulation layer such as e.g. SiO_2. The p region and the n region can have either a constant or a graded

doping; the graded doping being preferable in either region if it is used as an on-state drift region.

As an example of a simple device within the scope of the present invention, Figure 2 of the accompanying drawings shows a simple silicon semiconductor pn junction diode as shown in Figure 1a but embedded in a dielectric material, that is to say the field shaping dielectric material is located adjacent both sides and bridging the pn junction and is capacitively coupled to the diode device electrodes. As shown in Figure 2, the dielectric is also coupled to the p+, p, n and n+ regions at both sides of the pn junction. The dielectric could instead be coupled to the p and n regions without being coupled to the diode contact (n+ and p+) regions or diode electrodes. The induced stretched edges of the pn junction depletion layer at reverse breakdown voltage are indicated, as in Figures 1a and 1b, with dashed lines.

The extent of the stretching of the pn junction depletion layer and the resulting amount of increase of the diode device reverse breakdown voltage are a function of the doping level of the semiconductor material. The p side and the n side of the pn junction may have the same doping level. Otherwise, the p and n sides may have different doping levels, and if there is a substantial difference then the depletion layer width is mainly determined by the side which is more lowly doped. The extent of increase in the breakdown voltage also depends on the relative widths of the semiconductor material and the field shaping dielectric material. Primarily the increase of the breakdown voltage of the semiconductor pn junction is caused by the difference of the dielectric constants of the semiconductor material and the insulating field shaping region material. The dielectric constant of, for example, silicon semiconductor material is about 11.7 to 11.9 compared with a dielectric constant of approximately 22 for Ta2O5 which is a suitable dielectric material for use as the field shaping region(s) in devices according to the present invention. Also, the breakdown electric field strength of the insulating/dielectric material is sufficient to withstand the electric fields occurring in the geometries of the device structures in accordance with the present invention; for example it is 3-5MV/cm for Ta2O5. The standard dielectrics silicon dioxide SiO2 and silicon

nitride Si3N4 used in semiconductor devices may also be used for the field shaping region(s) in devices according to the present invention. SiO2 has a dielectric constant of 3.9 and a breakdown strength of 12-15 MV/cm. Si3N4 has a dielectric constant of 7-9 and a breakdown strength of 10-11 MV/cm which is much higher than the 0.2MV/cm breakdown field strength for semiconductor silicon. For a doping level of 1E17, which in this example is the same for the p and the n regions,, a width of the semiconductor silicon of 0.4 micron and the same width of each of the two field shaping dielectric regions, the breakdown voltage of the silicon semiconductor diode device shown in Figure 2 having Ta2O5 dielectric goes up from 21.4 Volt to 36 Volt.

The spreading of the voltage, that is to say the stretching of the electric field and the depletion layer across the pn junction, caused by the dielectric in the diode device shown in Figure 2 is clearly visible by comparing the equilines of voltage at breakdown for width-0.4 micron as described above as shown in Figure 3A (breakdown voltage = 36 Volt) with the equilines in the geometry of the Figure 1a device as shown in Figure 3B (breakdown voltage-21.4 V). In Figures 3A and 3B the pn junction is at 4.0 micron on the vertical axis, the p+ region is from 0.0 to 0.2, the p region is from 0.2 to 4.0, the n region is from 4.0 to 8.0 and the n+ region is from 8.0 to 8.2. The vertical height of the Figure 2 device as shown in Fig. 3A was chosen higher than was actually needed; a ~~total height on the vertical axis from 2.5 micron to 5.5~~ micron would have been sufficient to demonstrate the effect.

Some explanation of the effect for the device of Figure 2 as shown in Figure 3A is as follows. This is a 2-dimensional capacitor with one plate in the p-region and another in the n-region (more precisely the capacitor plates are distributed: the plates are at a larger distance at larger voltages). The voltage distribution and the field lines around the capacitor plates are a function of the materials (the geometry and their dielectric constants) around the capacitor plates. A simple example is a flat plate capacitor in which a high k dielectric is inserted between the plates: assuming the same charge at both plates the voltage goes down at the plates. The same type of behaviour holds for the semiconductor diode: introducing the high-k dielectric parallel to the junction

and assuming the same charge at both sides will lead to a lower voltage over the diode. Now we can increase the applied voltage up to the point where it was in the beginning. For this action extra charge in the depletion layer, thus a thicker depletion layer is needed. As a consequence a lower field will be at the junction at the same reverse bias. This will result in a higher breakdown voltage.

In a modification of the device shown in Figure 2, moving the junction upwards (so completely replacing the P by N) leads to a breakdown voltage of 15 Volt without embedded dielectric and 28 Volt with embedded dielectric (again with 0.4 micron wide silicon pillars embedded in 0.4 micron wide dielectric pillars). As a consequence of this modification the capacitive coupling is stronger and thus the depletion layer widening will be stronger in the lowly doped n-part. Because the depletion layer is wider in the lower doped part and it is possible to extend the depletion layer in this lowly doped part more easily also by this capacitive coupling one wants to enhance the effect by a tighter coupling. This is achieved by bringing the voltage from the p+ side closer to the n+ side. Thus the n-region is the piece of material with high resistivity and sustaining the high voltage. So it can also be used in MOSFET's.

A summary of simulated results for a doping of 5E16 and a doping of 1E17 in the diode shown in Figure 2 is given in the for both 2-sided and 1-sided junctions, that is to say with the dielectric adjacent both sides of the pn junction as is shown in Figure 2 and adjacent only one side of the junction as is also possible within the scope of the present invention, in the plots shown in Figure 4 of the accompanying drawings.

These results lead to the following implementation proposal:
Etch trenches crossing the diode junctions and fill these with an insulating material, preferably with a high dielectric constant (e.g. Ta2O5 having a dielectric constant >20; a liner of SiO2 for passivation of the silicon (2nm was used in the results/plots given above). Extra charge (so a wider depletion area) is needed for building up the critical electric field and thus a higher breakdown voltage results. The etching can be done in stripes but it would be

even better to etch trenches as either hexagonal or square meshes because then the spreading of voltage is stronger because an even higher charge and thus a wider depletion layer is needed at the same voltage. This mesh, or cellular, arrangement provides a larger area/volume ratio; having a larger area covered by high-k gives a stronger capacitive coupling, thus a stronger widening of the depletion layer (a better "RESURF") and thus a higher breakdown voltage.

In accordance with the invention, the concept described above in relation to a semiconductor diode device could be used in any other device with reverse biased junctions such as bipolar junction transistors and MOSFET's for giving a better trade-off between forward voltage drop, that is to say on-resistance, and breakdown voltage. E.g. in MOS devices as high as possible doping in the drain extension is attractive for on-resistance but the required breakdown voltage limits the doping level. By using insulating materials, preferably with a high dielectric constant, for the field shaping region adjacent and possibly bridging the pn junction this limitation is less strict. This adjacent field shaping region could be vertical e.g. in trenches, but also lateral e.g. for edge termination of junctions. Also in SOI devices one could use the mechanism either at the top side or at the bottom side by replacing the oxide layers by high-k layers or a sandwich of oxide and high-k layers; this configuration with the complete oxide replaced by high-k is shown in Figure 5.

In all devices within the scope of the present invention the higher the dielectric constant of the field shaping insulating material is, the higher the beneficial effect on the breakdown voltage. That is to say, if the field shaping insulating/dielectric material has a higher k value then the stretching of voltage equilines in the electric field in the field shaping material in the region adjacent to the semiconductor pn junction is greater and thus the maximal electric field is lower (the electric field is more relaxed) and the correspondingly induced stretching of the electric field and the pn junction depletion layer in the semiconductor material is greater and hence the breakdown reverse voltage of the pn junction is greater. The greater the k value of the field shaping material the thinner the region of this material can be to achieve a given increase in the

breakdown voltage of the semiconductor pn junction. Tantalum oxide Ta2O5 (k value approximately 22) is a preferred material for the field shaping region. Other insulating materials well known in silicon semiconductor technology such as silicon dioxide Si02 (k approximately 4) and silicon nitride Si3N4 (k approximately 8) could be used for the field shaping region in devices according to the present invention but this region would have to be much thicker than for Ta2O5 in order to achieve the same increase in breakdown voltage of the adjacent pn semiconductor junction. Since the dielectric field shaping region does not conduct any current, a thinner higher k field shaping region/layer leads to higher efficiency because more parallel diode/transistor cells can be present in a given device area with a consequent smaller on-resistance of the device. Other dielectric materials which could be used for the field shaping region in devices according to the present invention and which have a k value greater than that for silicon nitride are for example aluminium oxide Al203 (k = 4.5 – 8.4), strontium titanate SiTi03 and barium titanate BaTi03 (k – 12 – 15). An example of a material with a much higher k value is CoTiO3 (k = 40). Dielectric materials with a k value greater than 8 are preferred for use as the field shaping region in accordance with the present invention.

Figure 6 of the accompanying drawings shows a planar gate vertical insulated gate field effect transistor semiconductor device in accordance with the present invention. The field shaping insulating region, which may be Ta2O5, is adjacent to the pn junction between the p body and the n- drain drift region and is capacitively coupled between a first capacitor electrode which is integral with the n+ drain region and a second capacitor electrode preferably consisting of highly doped poly silicon or metal which is adjacent the p body region and source region of the device and at the same potential as these two regions. The second capacitor electrode could alternatively be the p body region or the source region itself. A metal or highly doped poly silicon second capacitor electrode, which is preferable because it results in stronger depletion in the n drain drift region, is preferably separated from the semiconductor silicon by a thin insulating layer (not shown). Figure 6A shows part of the

device of Figure 6 on an enlarged scale to illustrate the effect of providing the Ta2O5 field shaping region. Figure 6A shows the equilines of voltage at the reverse breakdown voltage (source to drain) of the device in the field shaping region and in the adjacent semiconductor region in the region of the pn junction. Hence the field shaping in the region of the pn junction which increases the breakdown voltage of the device is limited to the depletion region. This corresponds to the depletion region stretching shown for a diode in Figure 3A discussed above. In the examples of document W001/59847 discussed above the field shaping extends across the whole of the drain drift region and also farther away to where the field shaping semi insulative conducting region contacts the silicon again.

The advantage of the arrangement of the present invention is that the field shaping region is insulating and is capacitively coupled and shapes only the depletion region and does not "shape" the electric field in the semiconductor material containing the depletion layer far outside the depletion region. In the arrangements of W001/59847 and co-pending UK Patent Application No. 0221839, which use semi-insulating material as the field shaping region, the field stretching is over the whole length of the semi-insulating layer and this induces a stretching of the depletion layer in the semiconductor having the pn junction far outside the original depletion region which enlarges its capacitance more than is necessary for the required increased breakdown voltage of the device. With the capacitively coupled insulating field shaping region according to the present invention the stretching is limited automatically because the depletion layer charge increase is determining the stretching so that there is a "feedback" adapting to the reverse bias. It is the use of an insulating field shaping region which avoids the (parasitic) extra current leakage present in the arrangement of W001/59847 and limits the field shaping to the depletion region. Because the effect of the insulating field shaping region is limited to the part of the semiconductor silicon where a depletion layer exists, the exact location of the beginning and ending of the field shaping region is less sensitive than for the W001/59847 arrangement. Thus in the device shown in Figure 6 the field shaping region

could extend up to the metal source electrode as the second capacitor electrode and so bridge the pn junction. In this case the field shaping region would be capacitively coupled to capacitor electrode regions which are not quite at the same voltages as those at the two sides of the reversed bias pn junction in the semiconductor region (that is the p body and the n drain drift region). The effect would therefore not be quite so strong but would still be satisfactory. An insulating layer could be provided between a second capacitor electrode metal contact and the semiconductor regions. In other devices within the scope of the present invention, for example the diode as shown in Figure 2, the insulating field shaping region, since it will not allow current flow, can be connected between two metal capacitor electrodes.

In the examples of a field effect device described in co-pending UK Patent Application No. 0221839 and discussed above, the field shaping region is described as being intrinsic semiconductor material, or being extrinsic semiconductor material which is lower doped than the drift region or being semi-insulating material; a substantially constant electric field is induced in the whole of the drift region by the field shaping region; and the first and second capacitor electrode regions adjacent the ends of the field shaping region have different electron energy barriers. By contrast, in a field effect transistor in accordance with the present invention, the field shaping material is an insulating material; the capacitor electrode regions at the ends of the insulating field shaping region may have but do not have to have different electron energy barriers; and, importantly, an induced substantially constant electric field in the drift region (that is the stretched electric field as shown in Figure 6A) is limited to the depletion region near the p body – drift region junction and does not extend along the whole of the drift region, that is to say that the capacitive field shaping is limited to the depletion layer width which is where the voltage drop occurs in the device.

Figure 7 of the accompanying drawings shows a trench-gate vertical insulated gate semiconductor device in accordance with the present invention. The field shaping insulating region, which may be Ta2O5, is adjacent to and also bridges the pn junction between the p body and the n- drain drift region

and is capacitively coupled between a first capacitor electrode which is integral with the n+ drain region and a second capacitor electrode which is the metal source electrode. It is to be noted that in the examples of field effect devices described in co-pending UK Patent Application No. 0221839 and discussed above, the field shaping region does not bridge the junction between the p body and the n-drain drift region. Figure 7A shows the voltage equilines at the source to drain breakdown voltage of the device in the field shaping region and in the adjacent semiconductor region across the pn junction.

In general terms, all the field effect transistor devices which have been described above as being within the invention of co-pending UK Patent Application No. 0221839 may be modified to be within the scope of the present invention essentially by substituting insulating/dielectric material for the field shaping region. The devices just described with reference to Figures 6 and 7 of the accompanying drawings are examples of such a modification which is mainly by such substitution. Thus in the devices shown in the present Figure 7, the second capacitor electrode could be a Schottky barrier region formed by a continuation of the source electrode metallisation.

An example of a lateral insulated gate field effect transistor device according to co-pending UK Patent Application No. 0221839 which is modified to be in accordance with the present invention is shown in Figures 8A and 8B of the accompanying drawings. The n+ source region, the n+ drain region and the n- drain drift region are underneath a top major surface of the device. A planar insulated gate having a gate dielectric layer and a gate conductive layer is above the top major surface. A p body channel-accommodating region is also underneath the top surface. A field shaping high k dielectric region is above the top major surface adjacent, that is near to, the pn junction between the p body region and the n drain drift region and separated from the drain drift region by thin insulating SiO2 region. A source metallisation electrode contacts the source region and extends over an insulation layer covering the gate conductive layer to contact a p+ region which is adjacent one end of the high k dielectric field shaping region and provides one electrode for capacitive coupling of the field shaping region. The p+ region could be omitted with the

source electrode being in direct contact with the field shaping region. An opposite electrode for the capacitive coupling of the high k field shaping region is formed by the drain drift region. The device may be made as illustrated using a silicon layer on insulating substrate (SOI) process involving a buried oxide layer on a substrate.

Figure 9 of the accompanying drawings shows a schematic representation of a bipolar transistor according to the present invention. The n+ emitter region, p+ base region, n collector drift region and n+ collector region are embedded in a two sided arrangement of field shaping high k dielectric/insulating regions which, under reverse voltage, stretch the electric field/depletion region at the base-collector junction and increase the reverse breakdown voltage.

In general terms, all the bipolar transistor structures disclosed in published patent application W003/015178 may be modified to be within the scope of the present invention essentially by substituting insulating/dielectric material for the semi-insulating field shaping region referred to as the gate region in W003/015178. An example of this is shown in Figure 10 of the accompanying drawings, which is a modification of the structure shown in Figure 3 of W003/015178.

In the bipolar transistor of Figure 10, a vertical structure has an n+ collector substrate with a plurality of mesas each consisting of an n drift region, a thin p type base layer, an emitter-base space charge region and an emitter region. Each mesa is surrounded by a trench, optionally separated from the mesa by a thin passivating SiO_2 insulating layer, and containing high k insulating/dielectric material as the field shaping region. A first capacitive coupling electrode for the field shaping dielectric is formed by the n+ collector region and a second capacitive coupling electrode for the field shaping dielectric is formed by a metal contact on top of the dielectric. The second capacitive electrode contact could alternatively be connected to the base or the emitter.

Figure 11 of the accompanying drawings shows another example of a silicon on insulator (SOI) structure in accordance with the present invention.

The semiconductor p and n regions which are shown forming a pn junction could just be a simple diode device, but could also be considered as incorporating a drift region such as the body and drain drift region of a field effect transistor or the base and collector drift region of a bipolar transistor. In the structure shown in Figure 11 voltages can be connected to the semiconductor regions and to the field shaping regions by contacts to the left hand side and right hand side of the structure as shown. The presence of a high k field shaping region at the rear side as well as the top side of the p and n semiconductor regions illustrates that the capacitive field shaping in accordance with the present invention can involve a three dimensional (non-linear) distribution of charge.

Figure 12 of the accompanying drawings shows a structure in which the high k insulating/dielectric field shaping region is used in accordance with the present invention for increasing breakdown voltage at the edge termination of a pn junction, that is the point at which a pn junction ends with a smoothed curve at a lateral surface. In accordance with the present invention a high k field shaping region on top of the lateral surface induces a higher radius of curvature of the depletion layer of the pn junction formed at the lateral surface (the depletion layer shown with a dotted line is extended to the dash-dot line) and hence the breakdown voltage of the pn junction is increased. The relevant reverse voltage applied to the pn junction is applied to contacts A and B or to contacts A and C. Because the high k field shaping region touches the p and n regions (directly as shown or capacitively via a thin insulator) it is automatically connected and capacitively coupled to the same voltage as applied to the pn junction. Such edge terminations, which can benefit from the present invention as shown in Figure 12, occur with nearly all pn junctions in a planar semiconductor device. Thus such a junction in a planar device can be a simple diode as shown in Figure 12 or e.g. a base-collector junction.

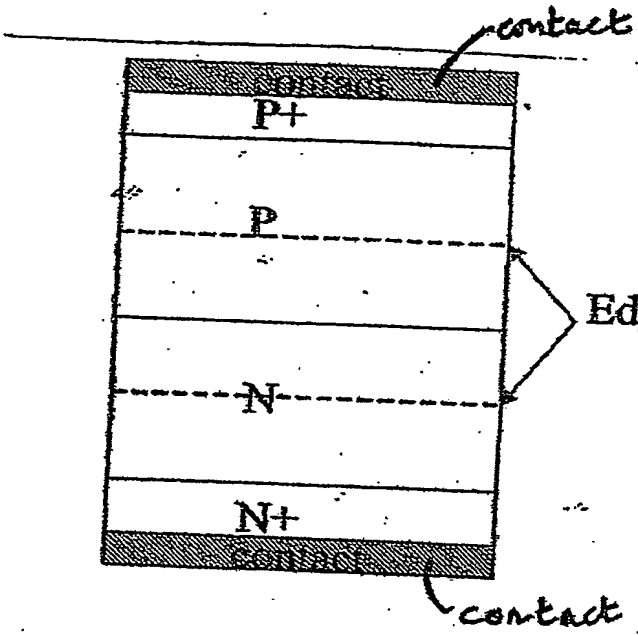

contact
contact
P+
P
Edges depletion layer
N
N+
contact
contact

Fig 1a

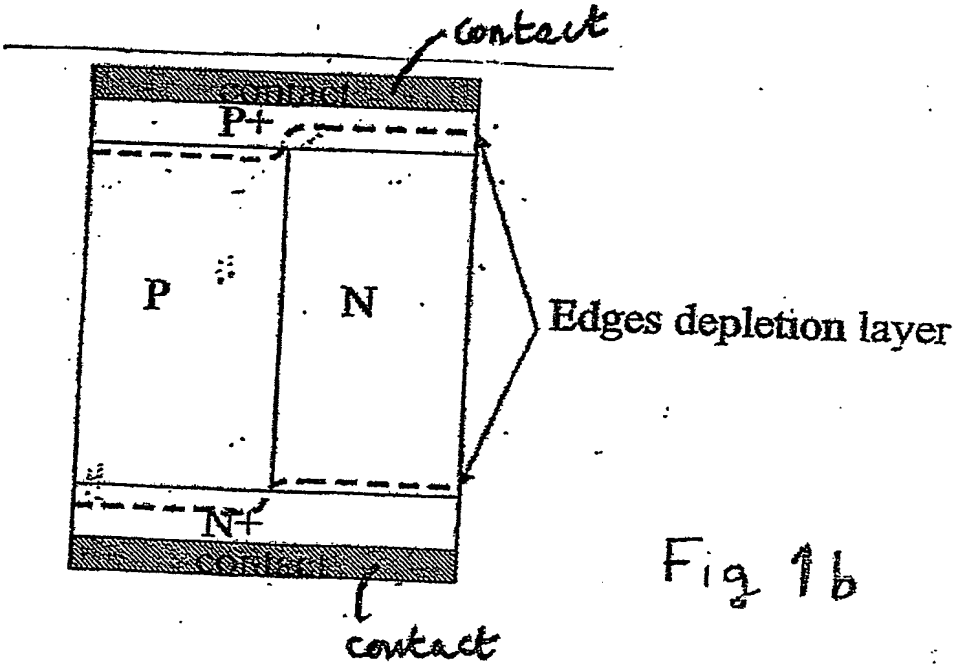

contact
contact
P+
P
N
Edges depletion layer
N+
contact
contact

Fig 1b

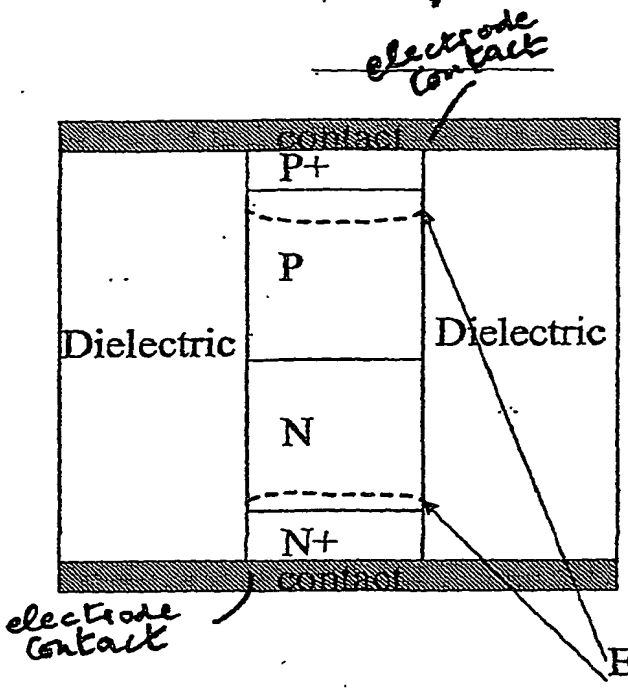
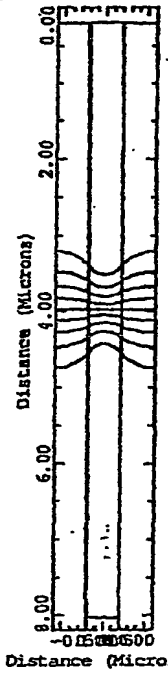
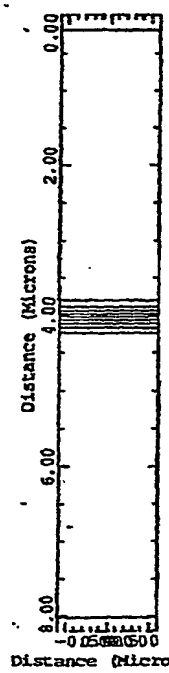


Fig. 2



Ta2O5 embedded silicon

Fig. 3A



Silicon only

Fig. 3B

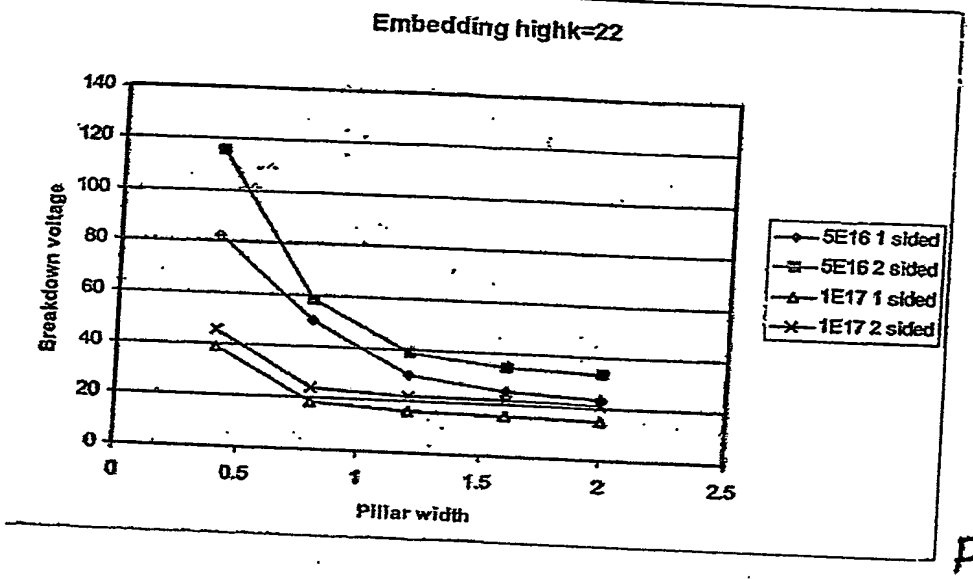

Embedding highk=22
Breakdown voltage
140
120
100
80
60
40
20
0
0
0.5
1
1.5
2
2.5
Pillar width
5E16 1 sided
5E16 2 sided
1E17 1 sided
1E17 2 sided

Fig. 4

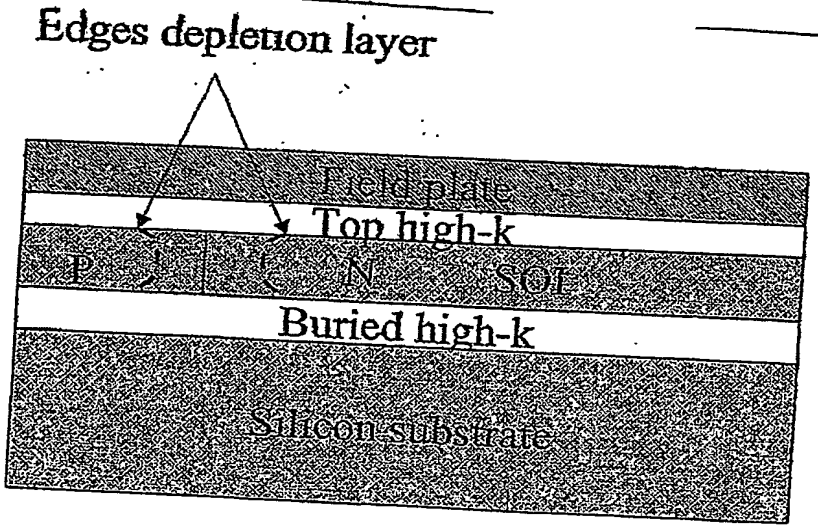

Edges depletion layer
Field plate
Top high-k
P
N
SOI
Buried high-k
Silicon substrate

Fig. 5

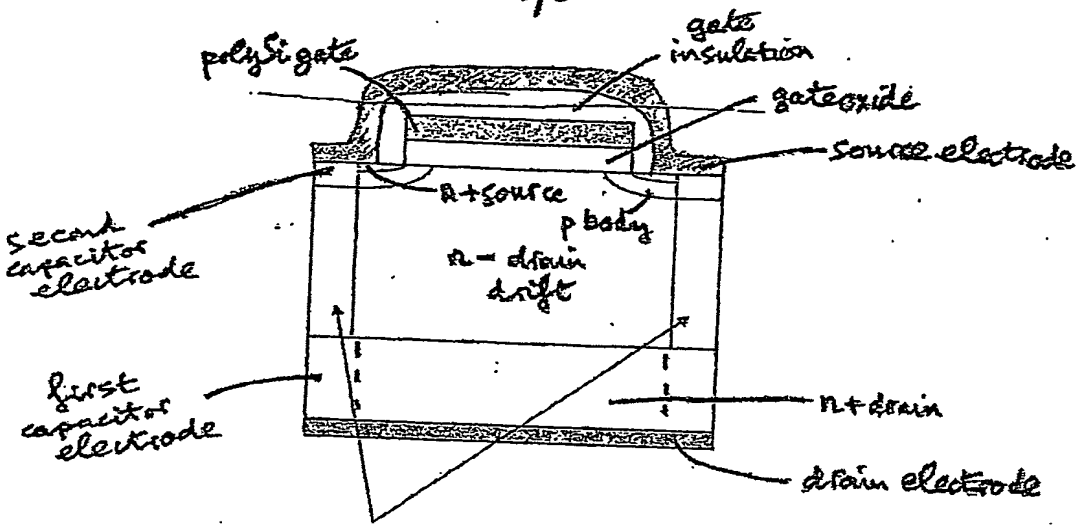

polySi gate
gate insulation
gate oxide
source electrode
second capacitor electrode
n+source
p body
n- drain drift
first capacitor electrode
n+drain
drain electrode
High-k

Fig. 6

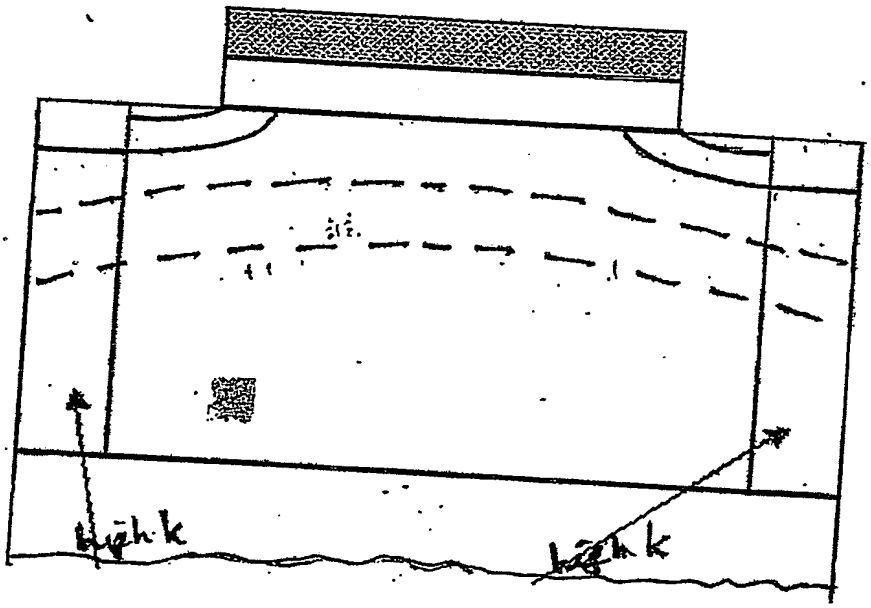

High-k
High-k

Fig. 6A

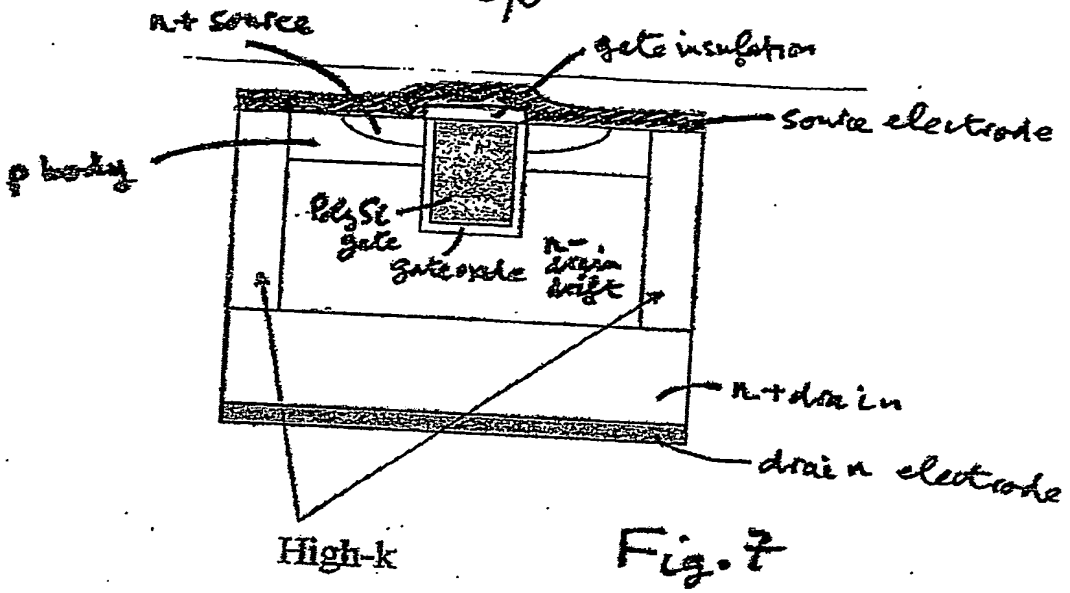

n+ source
gate insulation
source electrode
p body
poly Si gate
gate oxide
n- drain drift
n+ drain
drain electrode
High-k

Fig. 7

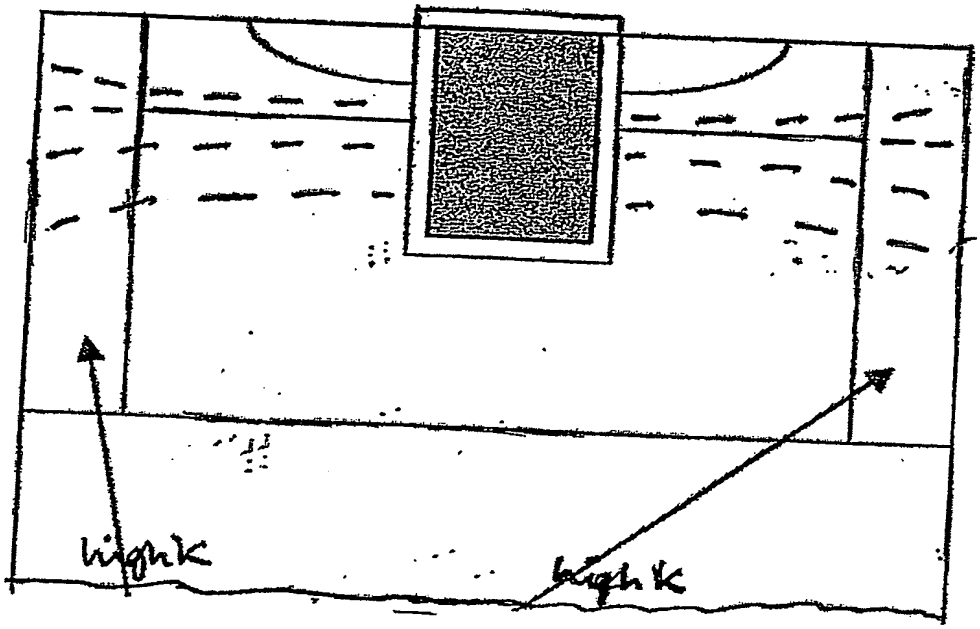

high k
high k

Fig 7A

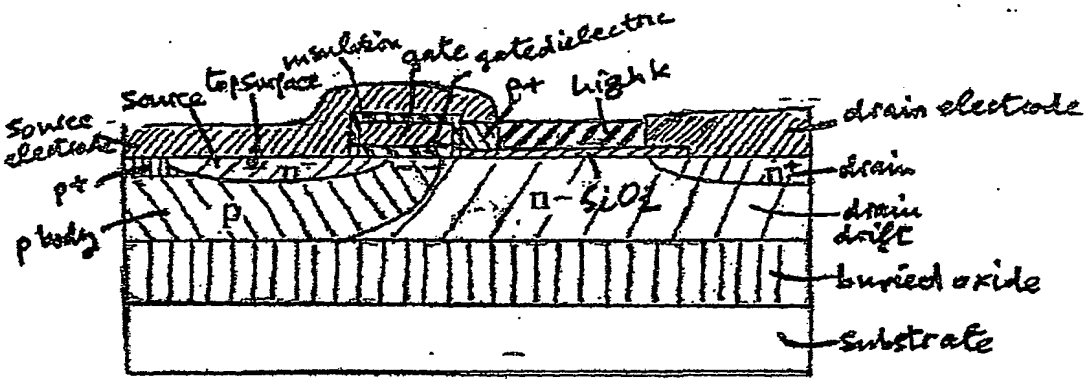

source electrode
source
top surface
insulation
gate
gate dielectric
p+
high k
drain electrode
p+
p body
p
n-
n-SiO2
n+
drain
drain drift
buried oxide
substrate

Fig 8A

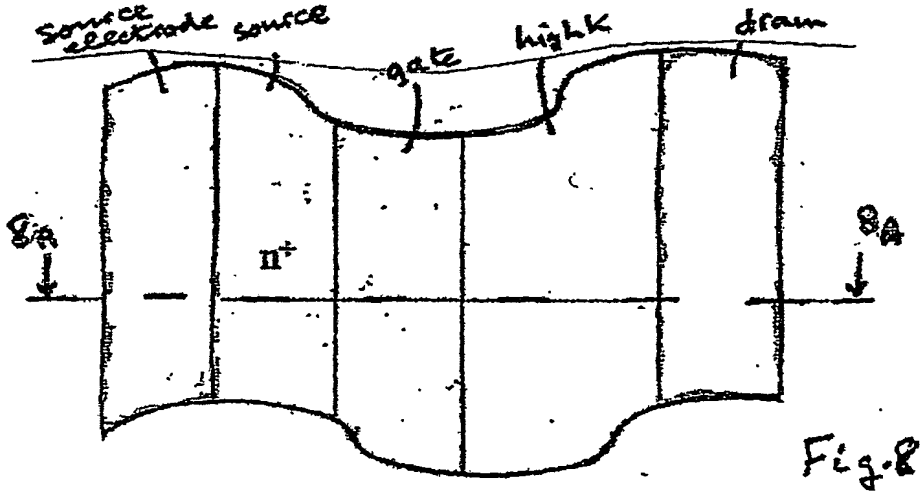

source electrode
source
gate
high k
drain
8A
8A
n+

Fig. 8B

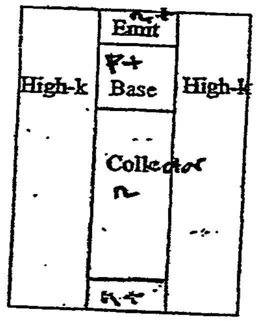

Emit
High-k
Base
High-k
Collector

Fig. 9

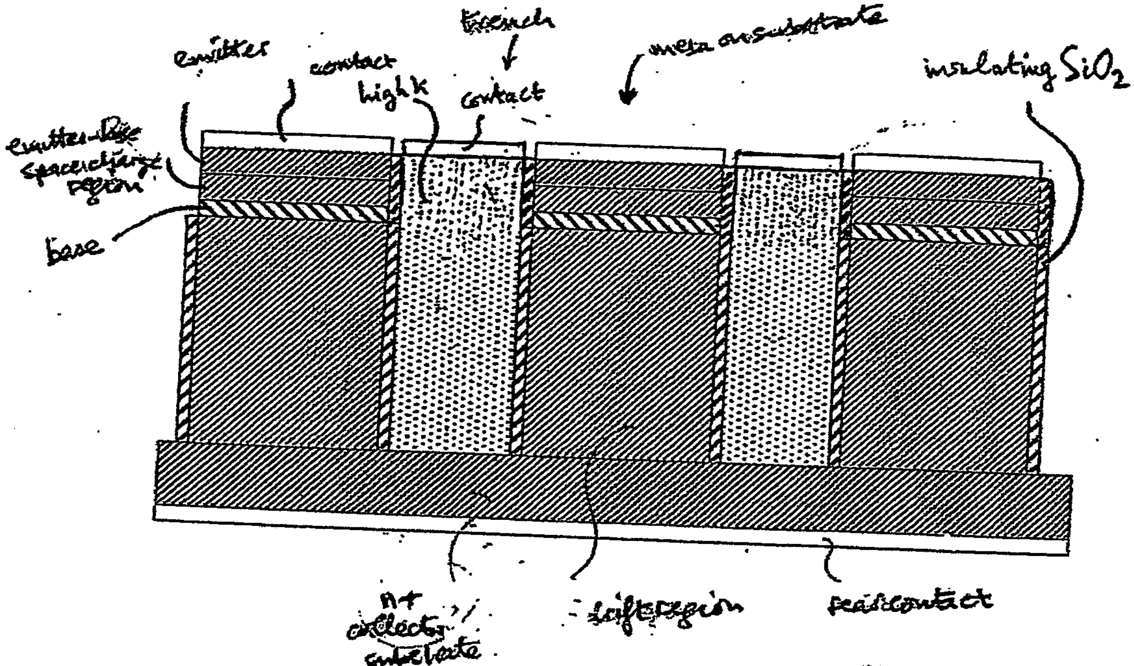

emitter
contact
high k
contact
insulating SiO2
base

Fig. 10

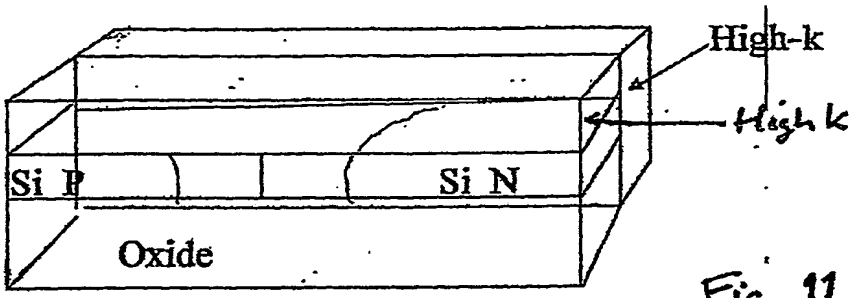

High-k
High k
Si P
Si N
Oxide

Fig. 11

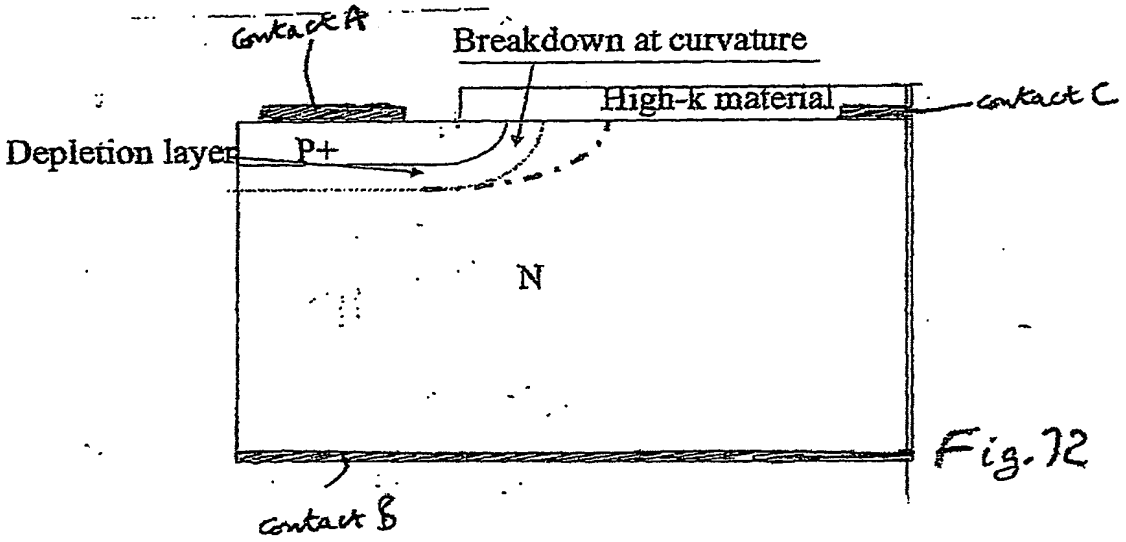

Contact A
Breakdown at curvature
High-k material
contact C
Depletion layer
P+
N
contact B

Fig. 12

PCT/IB2004/001527